(12) UK Patent Application (19) GB (11) 2 074 807 A

(21) Application No 8111005
(22) Date of filing 8 Apr 1981
(30) Priority data
(31) 143569
(32) 25 Apr 1980
(33) United States of America (US)
(43) Application published 4 Nov 1981
(51) INT CL³ G01S 13/52
(52) Domestic classification H4D 265 271 318 36X 402 40X 418 460
(56) Documents cited
GB 2044034
GB 1583829 ≡ US 4117538A
GB 1522181
GB 1362785
GB 1312945
GB 1192290
GB 1144456
GB 1092209
GB 1091868
(58) Field of search H4D

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(54) M.T.I. radar processor

(57) For moving target indication, in a three-pulse system, the radar returns to a rotating antenna 64 are detected (74), range sampled (76) and converted (80) to digital words in both in-phase (I) 70 and quadrature (Q) filters 110. The digital words following first and second pulses are stored in stores 82, 84 and fed with the words following the third pulse to three velocity filters 26, 28, 30 with different patterns of weighting coefficients for A, B and C channels corresponding to the three pulses. Filter 26 producing a signal F1 corresponds to a conventional MTI filter. The other filters for F2 and F3 have orthogonal weights so that noise is uncorrelated. The I and Q F_1 signals are squared (112) and summed (114) with conversion to logarithms to provide an output F_1 signal fed to video output circuits 116, the F_2 and F_3 signals being similarly treated. F_1 also updates a leaky bucket clutter map store 32 whose contents are subtracted above zero, 20 dB and 40 dB thresholds respectively from the F1, F2 and F3 signals before these are combined and converted back to a video output for a PPI display 54.

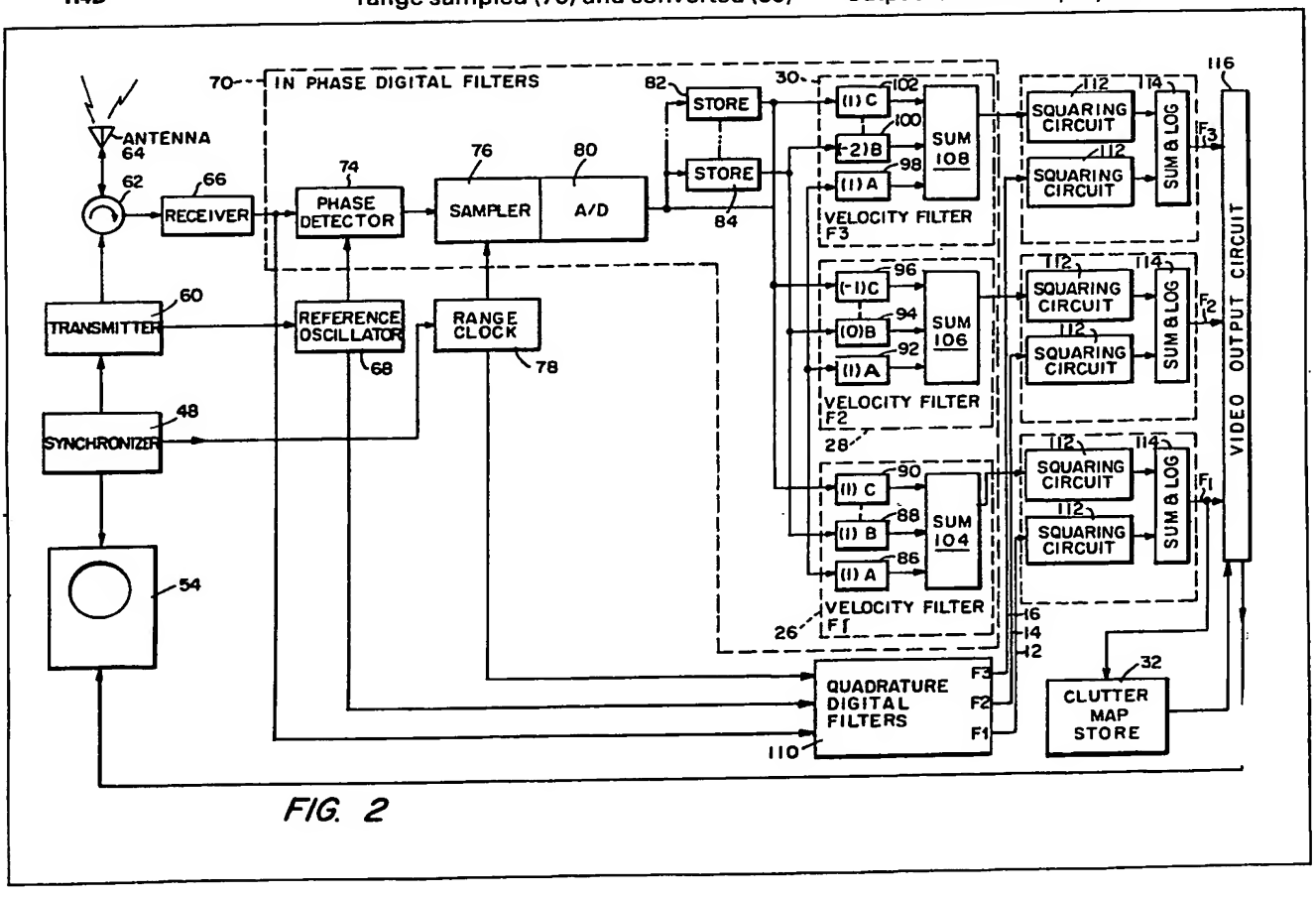

FIG. 2

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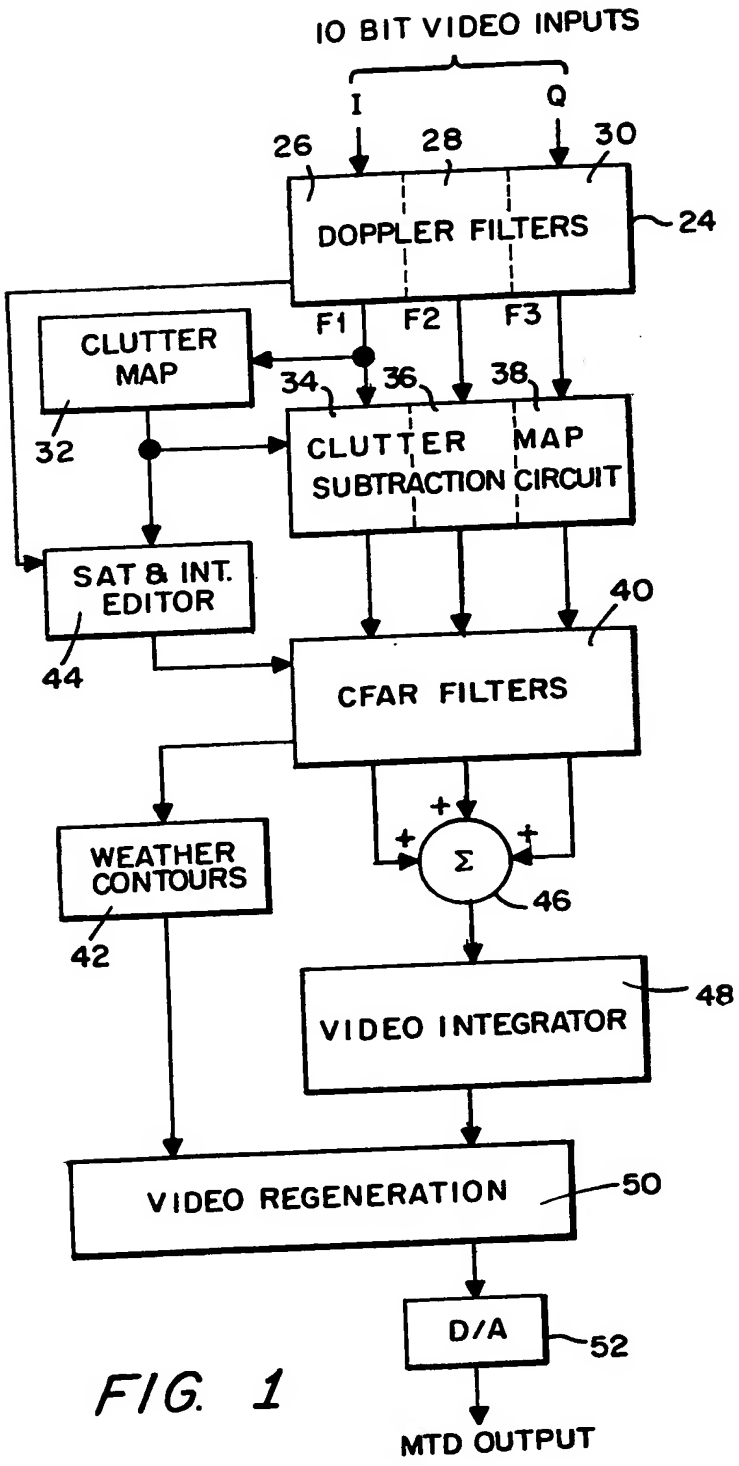
10 BIT VIDEO INPUTS
I
Q
26
28
30
DOPPLER FILTERS
24
F1
F2
F3
CLUTTER MAP
34
36
38
32
CLUTTER MAP SUBTRACTION CIRCUIT
SAT & INT. EDITOR
44
40
CFAR FILTERS
WEATHER CONTOURS
42
+
+
+
Σ
46
VIDEO INTEGRATOR
48
VIDEO REGENERATION
50
D/A
52
MTD OUTPUT

FIG. 1

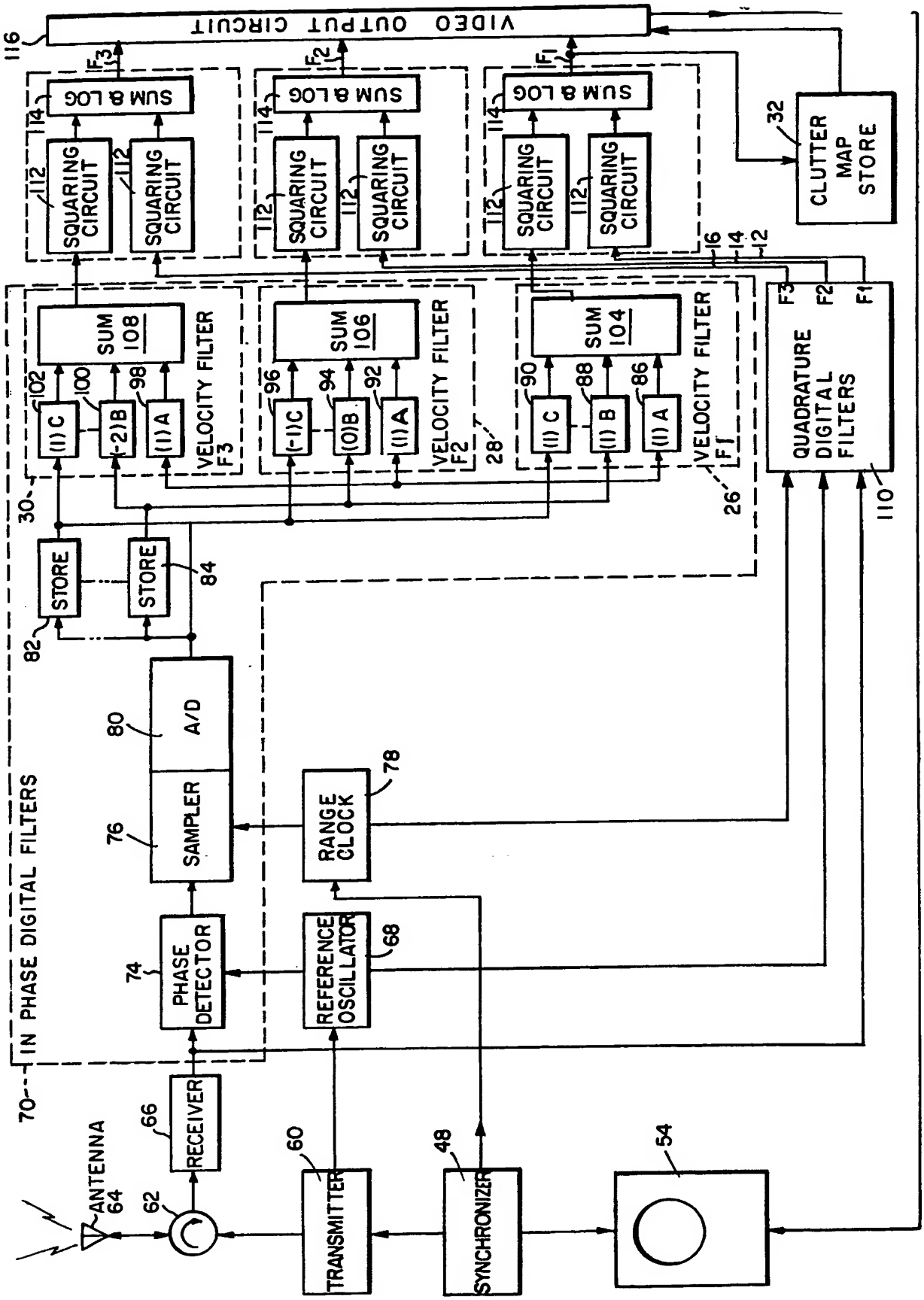
VIDEO OUTPUT CIRCUIT
116
SUM & LOG
SQUARING CIRCUIT
112
114
CLUTTER MAP STORE
32
VELOCITY FILTER F3
VELOCITY FILTER F2
VELOCITY FILTER F1
SUM 108
SUM 106
SUM 104
(1) C
(-2) B
(1) A
(-1) C
(0) B
(1) A
(1) C
(1) B
(1) A
102
100
98
96
94
92
90
88
86
QUADRATURE DIGITAL FILTERS
F3
F2
F1
110
16
14
12
28
26
30
STORE
82
84
IN PHASE DIGITAL FILTERS
70
A/D
80
SAMPLER
76
RANGE CLOCK
78
PHASE DETECTOR
74
REFERENCE OSCILLATOR
68
RECEIVER
66
ANTENNA
64
62
TRANSMITTER
60
SYNCHRONIZER
48
54

FIG. 2

2074807

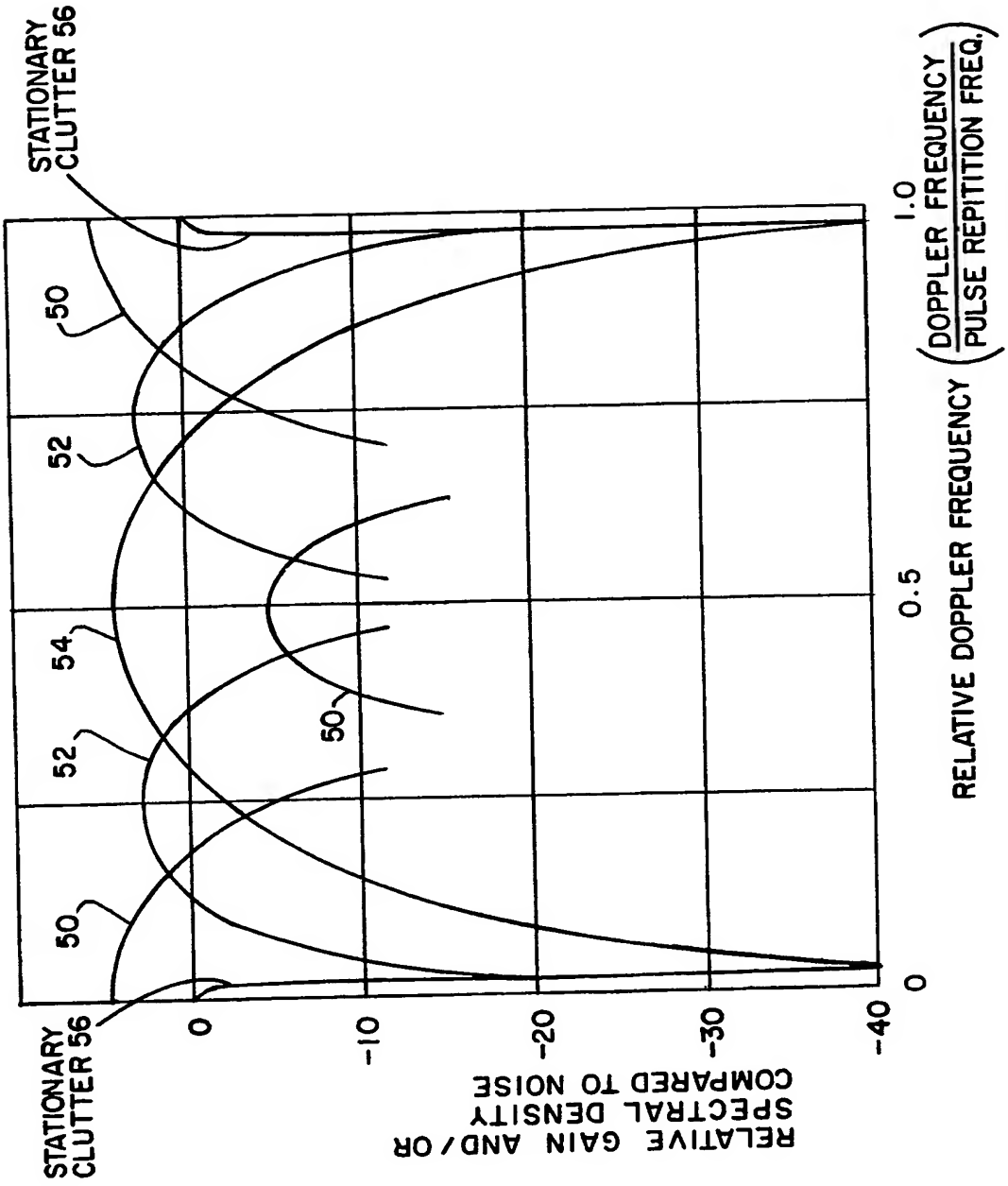

FIG. 3

SPECIFICATION

Radar processor

Moving target indicator systems have generally required the processing of signals from several successive sweeps to produce sufficient indication of differences between moving targets, particularly at low velocities. Alternatively, expedients such as utilizing weighting factors or weighting received ech signals as a function of range disclosed in U.S. Patent No. 4,117,538, summing composite video signals from present range sweeps and predictions of composite videos of such range sweeps have been used with digital techniques for improving moving target indicating systems.

In contrast to such prior art, the processor according to the invention is defined in claim 1 below.

Thus, sequencies of digital words can be derived from received signals, which are phase related to a reference signal, and weighted with coefficients which are functions of target velocities. Sums of the weighted sequencies may then be displayed.

More specifically, in carrying out the invention, a transmitter transmits pulses at any desired repetition rate and produces a reference signal which preserves the phase coherence of the transmitted signals. Received echo signals from targets are sampled for succeeding time periods following the transmitted signal to produce signals whose phase is compared with the phase reference and digitized outputs are produced and stored for succeeding transmitted pulses which, due to rotation of a directional antenna transmitting the pulses, produce slightly different echo signals. Signals from the same range or time delay from the transmitted signal, for three successive transmitted pulses are extract from the storage means or directly from the receiver to be submitted with appropriate weighting. The output of the summing system is then displayed on a display synchronized with the transmitted pulses to produce any desired display such as a plan position indicator. This invention further enables rejection of clutter returns which are larger than a predetermined threshold for each of the outputs from the summer corresponding to a velocity channel. Specifically all signals can be rejected as the comparison of the sum of the squares of the in-phase and quadrature phase components of a range sample when the magnitude is substantially different from such a sum for the same range of a second interpulse system.

Means may be provided for storing a sequence of summed outputs of the different velocity channels during the final interpulse period of the three interpulse period group and outputting the sequence a plurality of times for display by a radar display more than once for each interpulse.

The invention will be described in more detail, by way of example with reference to the accompanying drawings, in which:

Figure 1 illustrates a multi-filter processor;

Figure 2 illustrates a radar system embodying the invention and including the processor of Figure 1; and

Figure 3 is a graph illustrating the response of the filters to stationary ground clutter.

Referring to Figure 1, a three-pulse moving target detection system comprises a radar receiver 66 which feeds in phase (I) digital filters 70 and quadrature (Q) digital filters 110. Only the details of the I filters are shown; the Q filters 110 are similarly constructed.

The I filters include a phase detector 74 whose output is sampled by a sampler 76. The samples are fed to a 10-bit analog-to-digital (A/D) converter 80. The input video is sampled at 1/16 nmi and the digital samples are fed to the inputs of a group of Doppler filters 24 (Figure 1) each comprising three filters 26, 28 and 30. The dynamic range of the video (noise level to limit level) is set to 50 db, and all signals are preferably processed linearly over this range.

The three filters 26, 28 and 30 (and the like filters of the Q filters 110) are three orthogonally weighted filters. The video signal f_1 from filter 26, f_2 from filter 28 and f_3 from filter 30 at any sampling range are related to the A/D output signals by the following equations:

$$f_3 = a + c - 2b$$
$$f_2 = a - c$$
$$f_3 = a + b + c$$

where a, b and c represent the 3 sweeps within each bath.

The responses to the doppler frequencies which result are shown in Figure 3. Curve 50 shows the frequency response F_1 of filter 26, curve 52 shows the frequency response F_2 of filter 28 and curve 54 shows the frequency response F_3 of filter 30. Curve 56 shows a typical spectrum of stationary target radar clutter.

The I and Q doppler filter outputs are combined in each of the filters 26, 28 and 30 by conventional squaring, summing, and conversion to logarithms, utilizing circuits described below in conjunction with Figure 2. The resultant magnitude expressed as an 8 bit logarithmic word is fed out as F_1, F_2 and F_3 from filters 26, 28 and 30. Subsequent processing is performed on these 8 bit digital words.

The zero doppler filter 26 (F_1) supplies a 65536 cell adaptive clutter map storage 32. The clutter map resolution may be, for example, 1.40625° in azimuth (approximately the 3 dB radar antenna azimuth beamwidth) and 1/256 of the radar instrumented range. Accurate indexing of the clutter map azimuth to the PRF is not necessary, providing the radar transmits six or more pulses in the time the antenna rotates one 3 dB azimuth beamwidth.

The clutter map 32 which, due to logarithmic magnitude storage has a wide dynamic range, then provides outputs for each range azimuth location which are the integrated value of F_1 output over several azimuth sweeps. The outputs are compared with preset thresholds in subtraction circuits 34, 36 and 38. The amount of each threshold is preferably adjusted to be equal to the expected improvement factor for each filter 26, 28 and 30. Thus, for F_1, filter 26, there is no improvement so the threshold is zero and all the clutter map signals are subtracted from the output of filter 26 in circuit 34. For F_2, the subtraction circuit 36 preferably has a threshold of approximately 20 dB since F_2, curve 52, intersects the clutter curve 56 at this leve. Similarly, the threshold of the subtraction circuit 38 fed by F_3 is set around 40 dB since F_3, curve 54, intersects the clutter curve 56 at around 40 dB. Thus, in a stationary radar using this filter system, clutter due to stationary targets can be subtracted out of each of a plurality of different filter responses to the extent that this clutter obscures the expected improvement provided by the filter. This is accomplished by subtracting that portion of the stored clutter for each output sampled from the filters 26, 28 and 30, which exceeds the threshold setting for that filter response. Thus, false alarms passing conventional constant false alarm rate filters 40 due to clutter exceeding the filter clutter suppression capabilities are eliminated and the full receiver dynamic range becomes available.

Although ground clutter has been removed from the signals at this point, weather clutter may still be present at each filter output. The weather clutter strength in each filter output is determined by the doppler velocity of the weather itself, and by its actual velocity with respect to the radar. If the weather is very slow moving, then the clutter map will remove it from the F_1 filter, but not the F_2 or F_3 filter, if the weather has sufficient doppler velocity.

To reduce weather clutter, each threshold filter output is passed through an averaging (range only) CFAR filter 40 which uses the average of the greatest of 8 cells on either side of the mid cell as an estimate of the local noise background.

The CFAR filters 40 have low loss and can remain permanently in the signal path. This has the advantage that in addition to reducing the weather clutter to noise level, the CFAR filters also tend to normalize any variations in the noise baseline caused by the clutter map thresholding the doppler filter outputs.

The output averages of the CFAR filters 40 are used by the weather contour circuit 42 to produce two levels of weather contours.

An interference editor 44 controls false alarms due to interference and saturation limiting clutter. It measures the sweep-to-sweep amplitude modulation of each return in each range cell in each group. If the amplitude variation exceeds the expected antenna scanning modulation, whether it is single pulse or limiting clutter, the signal at that range is blanked in that group.

The three doppler filter outputs (F_1, F_2 and F_3), after being automatically normalized by the clutter map 32 and passed through separate CFAR filters 40, are merged into one signal in a combiner 46 and the resultant signal is anti-logged in a video intergrator 48 to produce a linear 8 bit signal which is then integrated by recursive integrator 48 which integrates the returns from successive three pulse groups as determined by a conventional synchronizer (not shown). Since the integrator 48 is operated in a linear fashion, the output signal dynamic range for the 8 bit signal is about 30 dB.

The output of integrator 48 supplies a video regenerator 50 which repeats the processed video ro raise its repetition frequency to a suitable value for display. Regenerator 50 supplies a d/a converter 52 whose output is a video signal supplied to intensity modulate a plan position indicator 54 in Figure 2.

Figure 2 shows radar equipment in which the processor of Figure 1 is incorporated. A pulse transmitter 60 generates short radio frequency pulses which are directed by a circulator 62 to an antenna 64 which radiates them towards a target. The signals reflected from the target are received by antenna 64 and are directed by the circulator 62 into the receiver 66 which amplifies them and down-converts them to an intermediate frequency.

A reference oscillator 68 generates a continous oscillation at the intermediate frequency whose phase is referenced to that of the transmitter. Such a system is well known and conventional.

The IF signal from the receiver 66 and the reference oscillation from the reference oscillator 68 pass into the in-phase section 70 of the processor where they are both applied to the phase detector 74. The output of the in-phase and quadrature-phase detectors 74 have amplitudes which follow that of the signal from the receiver, multiplied by the cosine and sine of the phase angle between the received signal and the reference oscillator signal. The outputs of each detector 74 are bipolar video signals which are passed to the sampling circuits 76 where, at times indicated by a range clock 78, samples of the video signal are passed to the analog-to-ditigal converters 80 which convert each sample into a digital word.

A sequence of the digital words from the A/D converter 80 occurs during the interpulse period following a transmitter pulse and this sequence is stored in a first store 82 which may be a conventional memory for 10 bit words, such as a random access memory on a shift register. The sequence of the digital words occurring in the interpulse period following the second transmitted pulse is stored in a second like store 84.

During the interpulse period following the last of the three transmitted pulses of the group, the digital words from the analog-to-digital converter 80 and from stores 82 and 84 are fed to the weighting networks 86, 88 and 90 of the F_1 velocity filter 26. Simultaneously, the digital words are fed respectively to weighting networks 92, 94 and 96 in the F_2 velocity filter 28 and to weighting networks 98, 100 and 102 in the F_3 velocity filter 30.

Weighting networks 86 to 102 provide weights to the digital words as follows:

86, 88, 90, 92, 98 and 102 are weighted	+1
94 is weighted	0
96 is weighted	−1
100 is weighted	−2

The digital words weighted by the networks 86 to 90 are summed in each velocity filter in summing circuits 104, 106 and 108 respectively. The weighting factors just given establish the abovementioned equations for f_3, f_2 and f_1.

The qudrature phase section 110 has components 74 to 108 which are identical to those in the in-phase section 70. The reference oscillator 68 supplies the phase detector in the section 110 with a reference signal which is 90° phase shifted from the reference signal supplied to the section 70 phase detector. Hence, the F_1, F_2 and F_3 outputs 12, 14 and 16 of the section 110 are in qudrature to the outputs of summers 104, 106 and 108 respectively.

The filters 24 contain six sequencing circuits 12 for squaring each of the two sets of digital outputs F_1 to F_3. The respective pairs of I and Q signals are then summed in summers 114 whose digital outputs are converted to logarithms to provide the digital outputs of the filters 26, 28 and 30. The video output circuit 116 contains the elements 34 to 52 of Figure 1.

In operation, the returns from a group of three radar pulses are processed coherently to produce three filtered outputs F_1, F_2 and F_3. For each three-pulse group processed, there is a single output from each of the three filters. The output from a zero doppler clutter map is subtracted from each of the three filter outputs above different predetermined threshold values for each filter to remove zero doppler return and to thus improve subclutter visibility. Groups containing interference or clutter entering saturation may be blanked by the circuit 44.

Averaging of CFAR in the range coordinate normalizes the signal levels in each filter before they are summed. The CFAR normalizing signals are also used to produce weather contours.

The three doppler filter outputs are formed after the in-phase and quadrature-phase components of three transmitted pulses have been collected and the three returns for one range sample are summed using three different sets of weights. The filter weights are preferably orthogonal to one another so that output noises are uncorrelated. Output F_3 is identical to that of a conventional three-pulse group single filter Moving Target Indicator. Both the real and quadrature signal components are processed identically, producing three real channel outputs and three quadrature channel outputs for each group of three input pulses. These signals rectified and combined to form a single output for each range sample.

The clutter map 32 consists of a leaky bucket pulse integrator for each range-azimuth resolution cell in the radar's coverage. The clutter map stores signals in cells which are controlled by control codes from the range clock 78 and by a standard azimuth encoder (not shown). Zero doppler returns are integrated for preferably about 1 beamwidth, of the rotating antenna 64, and the integrated value is stored in the clutter map 32. This operation synchronizes the map to the antenna, keeping the resolution cells on the map fixed in azimuth. The clutter map leaky bucket integrator sums F_1 over 8 to 10 azimuth scans of the antenna 64 for each cell of the map 32. Map 32 then supplied the signal to be subtracted from the zero doppler channel. For any selected range gate and beam position, this signal preferably is the largest map value taken from three by three grid of points about the cell of interest. This operation minimizes false alarms in the vicinity of large point clutter.

The map output is also compared with subclutter visibility thresholds, one for each doppler filter. When the map output is larger than the threshold, the difference between the map and the threshold is subtracted from the appropriate doppler channel. This operation provides a means of regulating the available subclutter visibility when radar stability has degraded.

The CFAR circuitry is a conventional range averaging CFAR. Range samples preceding and following the sample of interest are summed and the larger sum scaled and subtracted from the cell of interest to normalise its signal level. These CFAR circuits, which are used in each filter channel, may also be used to produce weather countours. Two levels of weather contours may be generated by comparing the largest of the three threshold signals to two fixed thresholds.

The particular circuit elements used herein may be simple weighting circuits and adders. Thus, inexpensive real time processing of radar signals can be achieved. With three pulse groups, several groups of pulses can hit every target using a high directivity radar antenna thereby improving azimuth accuracy with high definition and reasonable antenna rotation rates.

Among possible modifications, other filter weighting value could be used and other storage structure could be used for digital words.

CLAIMS

1. A radar processor, comprising means for deriving signals from directively radiated groups of three radar pulses in which the interpulse periods in each group are equal; a phase detector for extracting components of received signals phase related to the pulses; means for sampling these components at intervals in range; means for storing the sequences of samples generated during sequential interpulse

periods in the group; a plurality of velocity filters; each of the filters having means for weighting each sequence of stored samples with weighting coefficients some of which are different for different velocity filters; and means for normalizing the outputs of different ones of the velocity filters as a function of the clutter passing through the different filters.

2. A radar processor according to claim 1, wherein the clutter normalizing means comprises means for integrating signals from the receiver for different ranges on successive pulses of the azimuth direction of the radar antenna and subtracting different amounts of the stored clutter from different filter outputs.

3. A radar processor according to claim 2, wherein the outputs of the velocity filters are exponential functions of the samples.

4. A radar processor according to claim 1, 2 or 3, wherein samples of the clutter are stored as exponential functions of the samples.

5. A radar processor according to any of claims 1 to 4, wherein samples of both in-phase and quadrature phase components of the samples are stored and the sum of the squares of the velocity filtered in-phase and quadrature phase samples of each of the range samples are produced.

6. A radar processor according to any of claims 1 to 5, wherein the means for storing the sequence of samples comprises means for digitizing the samples and storing summed outputs of the velocity filters during the final interpulse period of each group of three interpulse periods.

Printed for Her Majesty's Stationery Office, by Croydon Printing Company Limited, Croydon, Surrey, 1981.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.